AMENDMENTS TO THE CLAIMS

Allowable claims 32-34 and 48-50 remain in the application. No claims have been amended. Claims 1-31 and 35-47 have been canceled, and no claims have been added. A listing of claims follows:

1–31. Canceled.

32. (Original) An apparatus comprising:

a memory unit to store a set of per-alignment state machines;

a memory controller coupled to the memory unit, the memory controller to access the set of per-alignment state machines;

a first deframing slice coupled to the memory controller, the first deframing slice having

a first set of buffers coupled to the memory controller, the first set of buffers to store a first set of states from a first subset of the set of per-alignment state machines,

a first set of logic coupled to the first set of buffers, the first set of logic to sync hunt a first signal with the first set of states and to update the first set of states,

a second set of buffers coupled to the first set of logic, the second set of buffers to store the updated first set of states, the updated first set of states to be written to the first subset of the set of per-alignment state machines; and

a second deframing slice coupled to the memory controller, the second deframing slice having

a third set of buffers coupled to the memory controller, the third set of buffers to store a second set of states from a second subset of the set of per-alignment state machines,

a second set of logic coupled to the third set of buffers, the second set of logic to sync hunt a second signal with the second set of states and to update the second set of states,

a fourth set of buffers coupled to the second set of logic, the fourth set of buffers to store the updated second set of states, the updated second set of states to be written to the second subset of the set of per-alignment state machines.

33. (Original) The apparatus of claim 32 wherein the first and second signal have different signal formatting.

34. (Original) The apparatus of claim 32 wherein the first deframing slice further comprises a third set of logic for a second signal format, the first set of logic being for a first signal format.

35-47. Canceled.

48. (Previously Presented) A network device comprising:

a first deframing slice having a first high bit rate signal format synchronization hunting logic and a first low bit rate signal format synchronization hunting logic;

a second deframing slice having a second high bit rate signal format synchronization hunting logic and a second low bit rate signal format synchronization hunting logic;

a memory to host a plurality of state machines;

a memory controller coupled with the first and second deframing slices and the memory, the memory controller to perform read and write operations between the low bit rate signal format synchronization hunting logics and the memory; and

a set of one or more machine readable media coupled with the first and second deframing slices, the set of machine readable media having stored therein a set of

instructions to cause the first low bit signal format synchronization hunting logic and the second low bit rate signal format synchronization hunting logic to simultaneously synchronization hunt low bit rate signals extracted from different high bit rate signals using the state machines stored in the memory.

49. (Previously Presented) The network device of claim 48 wherein the low bit rate signal format is DS-1.

50. (Previously Presented) The network device of claim 48 wherein the state machines are per-alignment state machines.